

Docket No.: P2001,0119

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : BERNHARD SELL ET AL.

Filed : CONCURRENTLY HEREWITH

Title : METHOD FOR FABRICATING A STORAGE CAPACITOR

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 4,589,193 (Goth et al.), dated May 20, 1986;

U.S. Patent No. 5,905,279 (Nitayama et al.), dated May 18, 1999;

U.S. Patent No. 5,760,434 (Zahurak et al.), dated June 2, 1998;

U.S. Patent No. 5,262,343 (Rhodes et al.), dated November 16, 1993;

U.S. Patent Application Publication No. 2002/0125521 A1 (Schrems), dated September 12, 2002 and corresponding PCT WO 01/20681 A1 (Schrems), dated March 22, 2001;

European Patent Application EP 0 967 643 A2 (Gambino et al.), dated December 29, 1999;

European Patent Application EP 0 981 164 A2 (Bronner et al.), dated February 23, 2000;

European Patent Application EP 0 495 991 A1 (Takenaka), dated July 29, 1992;

PCT WO 01/17014 A1 (Sell et al.), dated March 8, 2001;

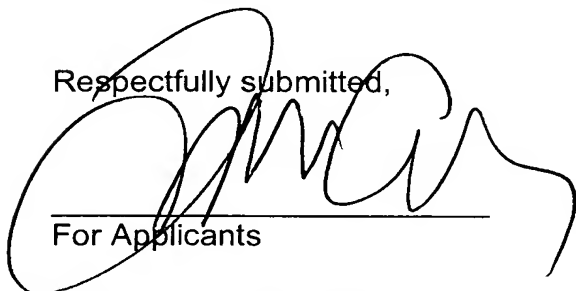
Patent Abstracts of Japan 63062371 (Akihiko), dated March 18, 1988;

Alperin, M. E. et al.: "Development of the Self-Aligned Titanium Silicide Process for VLSI Applications", IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 1, February 1985, pp. 61-69;

Yamada, K. et al.: "A Deep-Trenched Capacitor Technology for 4 Mega Bit Dynamic Ram", IEEE, IEDM 85, 29.3, pp. 702-705.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,



For Applicants

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Date: August 26, 2003

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Attorney Docket No.: P2001,0119 Appl. No.: _____ Applicant: BERNHARD SELL ET AL. Filing Date: August 26, 2003 Group Art Unit: _____			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	4,589,193	5/20/86	Goth et al.			
	B	5,905,279	5/18/99	Nitayama et al.			
	C	5,760,434	6/2/98	Zahurak et al.			
	D	5,262,343	11/16/93	Rhodes et al.			
	E	2002/0125521 A1	9/12/02	Schrems			
	F						
	G						
	H						
	I						
FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J	0 967 643 A2	12/29/99	Europe			
	K	0 981 164 A2	2/23/00	Europe			
	L	0 495 991 A1	7/29/92	Europe			
	M	01/20681 A1	3/22/01	WIPO			
	N	01/17014 A1	3/8/01	WIPO			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
		Alperin, M. E. et al.: "Development of the Self-Aligned Titanium Silicide Process for VLSI Applications", IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 1, February 1985, pp. 61-69					
		Yamada, K. et al.: "A Deep-Trenched Capacitor Technology for 4 Mega Bit Dynamic Ram", IEEE, IEDM 85, 29.3, pp. 702-705					
EXAMINER				DATE CONSIDERED			
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EXAMINER INITIALS	A	PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT							
	J	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J	63062371	3/18/88	Japan			
	K						
	L						
	M						
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		

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